Demonstration of A Time-domain Wavelength Interleaved Network Prototype without Optical Buffers and Fast Switches in the Core Nodes

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Abstract: We demonstrate a packet-switched network prototype without the needs for optical buffers and fast switches in the core. This network architecture is based on time-domain wavelength interleaving of data packets.

OCIS codes: (060.2330) Fiber optics communications; (060.4250) Networks

1. Introduction

Sub-wavelength switching in optical domain has gained significant interest due to its potential in lowering the transmission cost and the capability to provide fine granularity to end users. Optical packet switching (OPS) and optical burst switching (OBS) have been proposed to improve the utilization of wavelength connections in transparent networking. In OPS, packets on the order of 100 ns from the input fibers are switched to the output fibers in the optical domain. This requires ultrafast optical cross-connects or switches for forwarding packets, and optical buffers for resolving packet contention. In OBS, depending on the protocols used for resolving burst contention, the network core nodes may or may not need optical buffering. However, OBS still requires fast optical switching capable of reconfiguration at microsecond timescale and the associated contention algorithm at each switch. Fast switching and optical buffering currently present significant technological challenges.

A Time-domain Wavelength Interleaved Networking (TWIN) with a mesh topology has recently been introduced as an efficient and cost-effective alternative to both OPS and OBS [1]-[3]. TWIN provides sub-wavelength granularity in a packet switching manner without the need for fast (microsecond or even millisecond) switch reconfiguration or optical buffering in core nodes. Also, TWIN performs efficient traffic grooming without resorting to electronic cross-connects, as is done in conventional TDM networks such as SONET/SDH [2]. This architecture consists of a simple core that is based on passive wavelength-selective switches (WSS) capable of routing incoming wavelengths to the appropriate outgoing ports (or fibers), and an intelligent edge utilizing fast tunable lasers to emulate fast switching of data in the core.

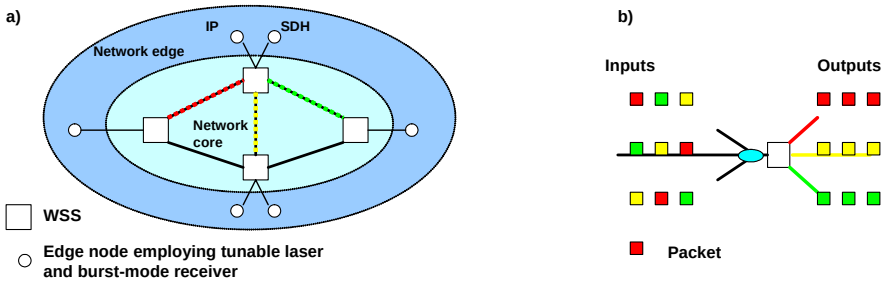

Fig. 1 a) TWIN architecture employing WSS based passive core nodes, b) Self-routing of packets in a WSS according to their wavelengths.

A sample TWIN network is shown in Fig. 1a. In a TWIN network, each source has a burst assembler which collects data units from clients, assembles them into bursts and then buffers the bursts for transmission to different destinations. Each source also has a fast-tunable laser for transmitting bursts optically. When a source has a burst to send to a given destination, the source tunes its laser to the wavelength uniquely assigned to that destination for the duration of the burst. When a destination receives a burst through its burst-mode receiver, it disassembles the burst into individual native data units upon conversion to electronic domain and then forwards them to appropriate clients. The simplicity of TWIN lies in the forwarding of bursts from one node to the next until they reach their intended destinations. The WSSs in the core makes the network core self-routing in that packet-forwarding relies on the wavelength rather than label/address lookup. Fig. 1b illustrates the switching principle in a 1x3 WSS where incoming bursts at one wavelength are switched to the same output port. Bursts are not buffered in the core, instead,

the bursts are scheduled in order to avoid contention at the destination [3]. Because the routes followed by the bursts form optical multipoint-to-point trees, there is no contention at intermediate nodes as long as contention is avoided at the destination.

In this paper, we experimentally demonstrate the *first* TWIN prototype employing a core node and three edge nodes to illustrate the basic operation. In particular, we demonstrate several important functions and features of the network architecture, including *self routing*, *fast wavelength switching*, and *data assembly* and *de-assembly*.

2. Architecture and modules

We built a testbed (Fig. 2a) including one core node employing a 1x2 WSS, one transmitter node at the edge equipped with a tunable laser, and two receiver edge-nodes operating in burst mode, as shown in Fig. 2b. The WSS directs two wavelengths from node 1 to node 2 and 3, respectively.

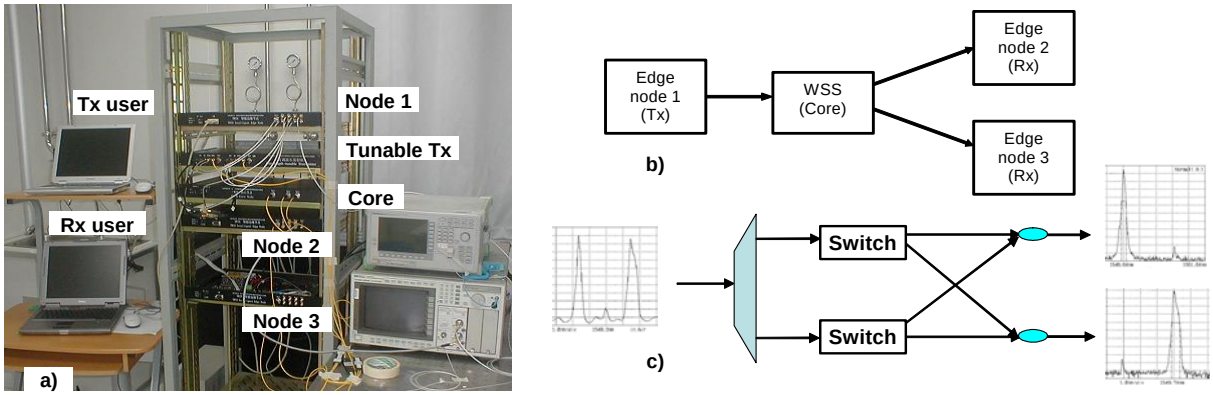

Fig. 2 a) TWIN testbed prototype, b) the architecture employing a core node and three edge nodes, c) the 1x2 WSS.

The 1x2 WSS is configured using an array waveguide grating (AWG) device, two mechanical space switches to re-configure the WSS, and the coupler for combining the signals. The AWG is a 40-channel device with 100-GHz spacing, but only two channels are used in this particular demonstration. The input signal can be routed to any desired output port. Fig. 2c shows the structure of the WSS and the optical spectra when signals of 1546.6 nm and 1549.7 nm are separated at the output ports of the WSS, respectively.

The edge nodes consist of transmitter and receiver parts. Data received from users are processed in an ingress queue, then assembled into bursts at 1.25 Gb/s with a 0011111 pattern added at the beginning of the burst as a synchronization symbol. No preamble bits are needed for the burst mode clock/data recovery (CDR) if the number of consecutive ‘0’s (guard time) is less than 100 bits. Therefore, in scheduling the network we put dummy bursts to fill empty slots, in order to relax the requirements on burst mode reception. This is achieved by using the DFB array containing two lasers for switching wavelengths, which send data and dummy bursts alternately. The DFB array is capable of multicasting function, which can output two wavelengths in our case. An FPGA (Altera EP2C35F484C7) generates parallel data to be transmitted at 125 Mb/s, bursts intended for different destinations are put in different queues. 8B/10B encoding is realized for the data in the FPGA. In addition, the FPGA also provides wavelength-control signals to switch the tunable transmitter, and the scheduling implemented in the FPGA is simply 1 by 2 switching with a duty cycle of nearly 50% for each burst in a period. The parallel data is then sent to a Serializer/Deserializer (SERDES, AMCC S2060) which outputs 1.25-Gb/s serial data with the synchronization symbol of 0011111. The burst switching speed is at bit level as wavelength selection is simply realized by on/off switching a DFB laser. At the receiver, the burst mode receiver consists of a photo detector, a fast automatic gain control (AGC), a limiting amplifier, and a SERDES of the same model as in the transmitter. The block diagram of the edge node is provided in Fig. 4a, while Fig. 4b shows the corresponding implementation where the tunable transmitter is placed in a separate box. In the edge node a MAC/PHY chip (Intel 82545) is used as Ethernet interface.

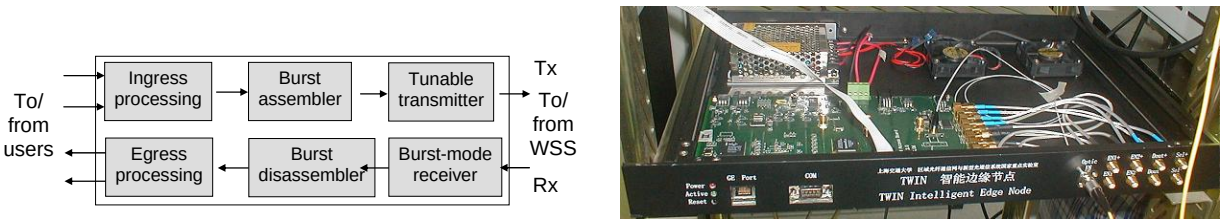

Fig. 4 a) the configuration of an edge node, b) a photo of the edge node (the tunable transmitter not included).

3. Experimental results

We first characterize the receiver performance by observing the recovered data and clock signals and measuring the sensitivity of the receiver. The bit rate is 1.25 Gb/s, and each data burst has a duration of 1948 bits with 100 '0's between two bursts. The scheduling is performed such that the traffic from the node 1 is 50/50 distributed to node 2 and 3, respectively, and dummy bursts fill empty slots to ease the clock recovery. If a long idle time between two bursts is present, the receiver would need a preamble in the beginning of a data burst to facilitate bit synchronization. Fig.5a shows that the recovered electrical clock is 125 Mb/s and the clock maintains during the guard time. Fig. 5b shows the recovered data at the receiver output. Fig 5c is a zoom-in picture of a burst starting with a '0011111' pattern as the frame start symbol.

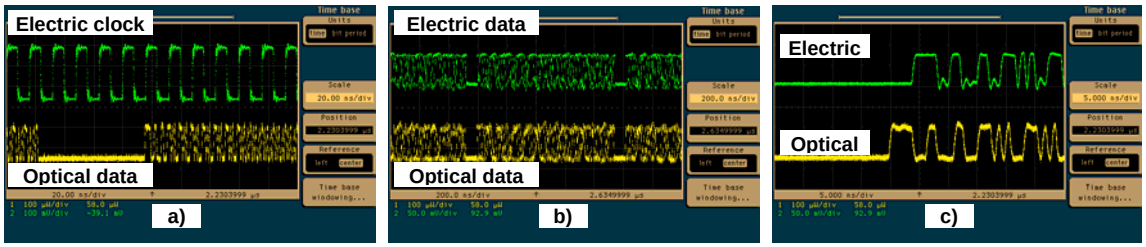

Fig. 5 a) Burst mode clock recovery, b) data recovery, and c) zoom-in picture of the received data.

Fig. 6a and 6b provide the BER measurements under two conditions: continuous data, and burst mode data with 100 'zero's between bursts. The results show a small sensitivity penalty of ~0.8 dB in the burst mode, mainly due to the performance of the CDR. We then observe the recovered parallel data from the FPGA. The screen capture of Fig. 6c shows the data transmitted at node 1 and the decoding process at node 2, respectively. The input 1.25-Gb/s 8B/10B data is converted to 8 parallel 125-Mb/s data, suitable for the FPGA operation.

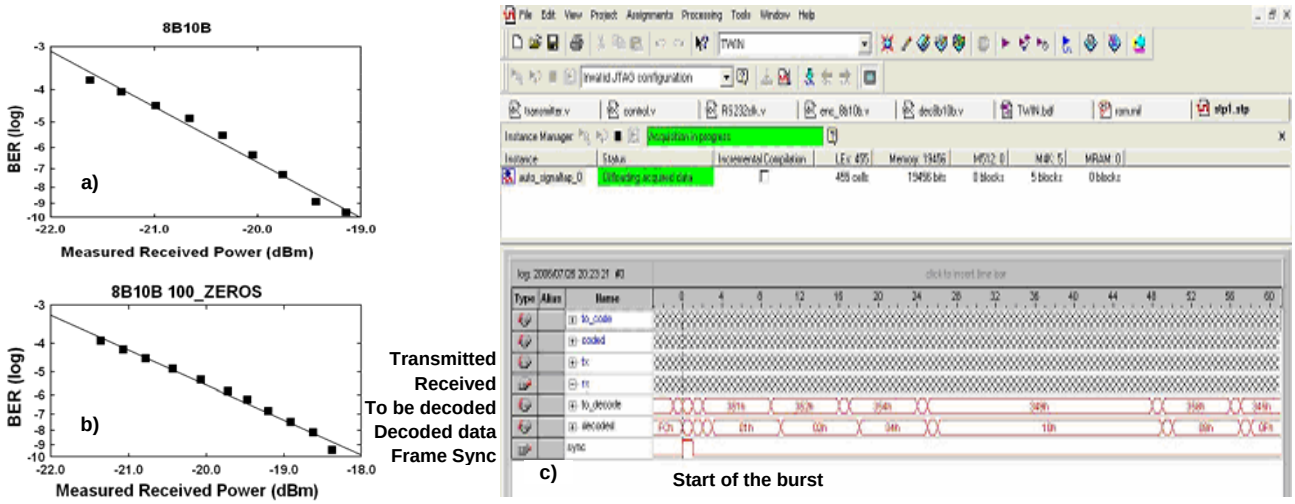

Fig. 6 a). BER measurement of the receiver with continuous data stream, b) burst mode performance with 100 '0's between bursts, c) screen capture of the data through the JTAG port of the FPGA.

3. Conclusion

We have demonstrated a TWIN prototype, which eliminates the needs for optical buffers and fast switching in core nodes. The experiment has shown some important basic functions of the network such as self-routing, fast wavelength switching, and data assembly/de-assembly.

Acknowledgement: This work was supported by the NSFC (60407008), the key project of Ministry of Education (106071), and the Fok Ying Dong Fund (101067).

References:

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